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09/548,826	04/13/2000	David E. Charlton	4076US(99-01860)	7750

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/548,826	Applicant(s) CHARLTON ET AL.	
	Examiner Cynthia Britt	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 13 April 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2, 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented for examination.

Drawings

The drawings are objected to because descriptive labels other than numerical are needed for figures 1-4. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, and 5 rejected under 35 U.S.C. 102(e) as being anticipated by Faulk Jr. U.S. Patent No. 6,256,756.

As per claims 1, and 5, Faulk Jr. teach a component with embedded memory is manufactured. The component includes a plurality of memory buffers and a processor. During self-test of the component, the processor performs testing of the plurality of memory buffers in order to detect bad memory locations. The processor places into a

free buffer list pointers to memory buffers from the plurality of memory buffers for which no bad memory locations have been detected. The error log is disclosed to be a non-volatile memory (abstract, column 3 lines 64-64, figure 1, claim 9).

Claims 9-19 rejected under 35 U.S.C. 102(e) as being anticipated by Di Zenzo et al. U.S. Patent No. 6,130,442.

As per claims 9-11, 15, 16, and 19, Di Zenzo et al. teach a method of testing a memory wafer, recording the failure information on the individual memory device in a nonvolatile memory. The failed information is used in the repair step and also in the later use of the memory, after the device is assembled IC (abstract, column 3 line 42 through column 4 line 56)

As per claim 12, Di Zenzo et al. teach that the nonvolatile memory can be an EPROM of Flash memory (column 3 line14-18, claims 4,5,7, and 8).

As per claims 13, 14, 17, and 18 Di Zenzo et al. teach that the information stored in the nonvolatile memory is used in a laser trimming stage and fuse blowing operations in order to repair as much as possible (column 3 line 57 through column 6 line 10, claim 3, figure 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2-4 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faulk Jr. U.S. Patent No. 6,256,756 in view of Webber U.S. Patent No. 6,274,395.

As per claims 2-4, and 6-9, and Faulk Jr. substantially teach the claimed component with embedded memory. The component includes a plurality of memory buffers and a processor. During self-test of the component, the processor performs testing of the plurality of memory buffers in order to detect bad memory locations. The processor places into a free buffer list pointers to memory buffers from the plurality of memory buffers for which no bad memory locations have been detected. The error log

is disclosed to be a non-volatile memory (abstract, column 3 lines 64-64, figure 1, claim 9). Not explicitly disclosed is that the nonvolatile memory is one of the following: EEPROM, EPROM, Ferro-electric device, flash memory.

However, in an analogous art, Webber teaches a method in which a memory device is fabricated having a nonvolatile memory for storing the locations of the failed memory devices. Webber teaches testing the device and recording the die pass/fail output information from the tested wafer on a nonvolatile memory Webber also discloses that the nonvolatile memory is a flash memory EEPROM device (column 4 lines 24-41, figure 2). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used a Flash memory EEPROM device as the nonvolatile memory disclosed by Faulk. This would have been obvious as suggested by Webber column 2 lines 10-23 in order to track the wafer die data.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,651,202 Phan

This patent provides a method and circuitry for providing memory fault information to and performing built-in self repair operations in an integrated circuit without the requirement of first performing a built-in self test procedure. In accordance

with the invention, a fuse array or other non-volatile memory device is provided to store information related to defective memory locations identified during the manufacturing process. (column 4 lines 6-14)

U.S. Patent No. 6,330,693 Lindsay

This patent employs a field programmable gate array ("FPGA") or hardware implemented look-up table for rapidly routing the error data received from an error compare circuit to an error catch memory in a manner such that the error data is stored in the error catch memory at physical addresses that correspond to logical addresses employed by the device being tested. As a result, the router circuit continually routes error data to particular physical locations in the error catch memory. A topological circuit, such as an FPGA, remaps the physical locations of the error data from the error catch memory to spatial locations for display on a bitmapped display device such as a CRT. Different programming technologies, such as anti-fuses, non-volatile memory elements, memory element controlled switches, etc., can be used in FPGAs. (column 3 lines 4-58 and column 8 lines 2-4)

U.S. Patent No. 6,115,828 Tsutsumi et al.

This reference teaches the failure address register includes a plurality of bit registers which correspond in number to the bits of the address of a memory cell. The failure address register stores the address of the failed memory cell. The failure address register preferably includes a PROM, like OTPROM (one-time programmable

ROM), or EPROM (erasable and programmable ROM), or a non-volatile memory, like NVRAM. (FIG. 5, Column 5 lines 14-22)

U.S. Patent No. 6,467,054 Lenny

This patent claims: A method of testing a storage device having an industry-standard interface, components and a non-volatile memory, the method comprising: receiving a test command via the industry-standard interface from a host computer; the storage device performing a test on one or more of the components according to the test command; the storage device identifying the failed component and a corresponding failure checkpoint of the test being performed, if a failure is detected by the storage device; and said storage device providing a pass/fail indication to the host and storing results from said test in the non-volatile memory, said results including the failed component identification and the failure checkpoint if a failure was detected. (claims 1 and 13)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner